Comprehensive Study on 2.5D Package Design for Board-Level Reliability in Thermal Cycling and Power Cycling

Interactive Poster Presenter: Shuai Shao, Yuling Niu, Jing Wang, Ruiyang Liu, Seungbae Park - Department of Mechanical Engineering, Binghamton University, Binghamton, NY 13902

E-Mail: sshao1@binghamton.edu

Abstract

2.5D packages have been widely used in electronics industry for high performance and product miniaturization. As Through-Silicon-Via (TSV) fabrication methods and multi-level assembly technologies get mature, 2.5D packaging becomes reliable and affordable. In this work, board-level life prediction was performed for a 2.5D Field-Programmable Gate Array (FPGA) assembly in both accelerated thermal cycling (ATC) and power cycling (PC). Finite element models were built and validated by warpage measurement. Solder fatigue life in PC was investigated by computational fluid dynamics (CFD) simulation and finite element analysis. Improved life prediction for PC was achieved by mapping temperature results from CFD model to finite element model.